WHAT IS CLAIMED IS:

1. A plasma display, comprising:

a panel;

at least one voltage source for supplying a sustain voltage to the panel;

an inductor for recovering an energy stored in the panel by a resonance phenomenon such that the recovered energy is reusable for driving the panel; and

first and second switches arranged, in parallel, between the inductor and the panel.

2. The plasma display as claimed in claim 1, wherein at least one voltage source comprises:

a first voltage source for charging the panel to a first polarity; and

a second voltage source for charging the panel to a second polarity different from the first polarity.

3. The plasma display as claimed in claim 2, further comprising:

a third switch for forming a conductive path between the first voltage source and the panel; and

a fourth switch for forming a conductive path between the second voltage source and the panel.

4. The plasma display as claimed in claim 1, further comprising:

a first diode connected between the first switch and the panel; and

a second diode connected between the second switch and the panel.

5. An energy recovering method for a plasma display, comprising:

forming a first electrically conductive path between a first voltage source and the plasma display using a first switch;

forming a second electrically conductive path between a second voltage source and the plasma display using a second switch;

forming a third electrically conductive path between the inductor and the plasma display using a third switch; and

forming a fourth electrically conductive path between the inductor and the plasma display using a fourth switch connected, in parallel, to the third switch.

6. The energy recovering method as claimed in claim 5,

shutting off a backward current from the plasma display using a first diode connected between the third switch and the plasma display; and

shutting off a backward current from the fourth switch using a second diode connected between the fourth switch and the plasma display.

7. A plasma display comprising:

a display having a plurality of electrodes and having a corresponding display capacitance between first and second nodes;

an inductor coupled to the second node and a third node;

a first switch coupled between the first and third nodes; and

a second switch coupled between the first and third nodes, the first and second switches being formed in parallel, wherein

a first current path is formed via the panel capacitance, the second node, the inductor, the third node, the first switch and the first node, and

a second current path is formed via the panel capacitance, the first node, the second switch, the third node, the inductor and the second node.

8. The plasma display of claim 7, wherein the direction of the first and second current paths are opposite directions.

9. The plasma display of claim 7, wherein the first current path charges the display capacitance from a first potential to a second potential and the second current path discharges the display capacitance from the second potential to the first potential.

10. The plasma display of claim 9, wherein the display capacitance is charge or discharged based on an LC resonance frequency.

11. The plasma display of claim 10, wherein the display capacitance is charged or discharged based on a non-LC resonance frequency.

12. The plasma display of claim 11, wherein an energy of the inductor current is increased prior to the discharging of the display capacitance or the energy is decreased prior to charging of the display capacitance.

13. The plasma display of claim 11, wherein during charging or discharging, the display capacitance is clamped before a stored energy of inductor reaches zero.

14. The plasma display of claim 7, wherein the first current path further comprises a diode coupled between the first switch and the first node.

15. The plasma display of claim 7, wherein the second current path further comprises a diode coupled between the first node and the second switch.

16. The plasma display of claim 7, further comprising:

a first clamping circuit coupled between the first and second nodes; and

a second clamping circuit coupled between the first and second nodes.

17. The plasma display of claim 16, wherein the first clamping circuit comprises a third switch coupled to the first node and a first potential via a first conductive path, and the second clamping circuit comprises a fourth switch coupled to the first node and a second potential via a second conductive path, wherein the first and second potentials are different.

18. The plasma display of claim 17, wherein the first potential is provide by a positive power source, and the second potential is provided by a negative power source.

19. In display panels having panel electrodes and corresponding panel capacitance between first and second nodes, an inductor coupled to the second node and a third node, a first switch coupled between the first and third nodes and a second switch coupled between the first and third nodes, the first and second switches being formed in

parallel, an energy efficient method of driving said display panels through the inductor coupled to the panel electrodes, comprising:

(a) discharging the panel capacitance through said inductor initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum through a first current path formed via the panel capacitance, the second node, the inductor, the third node, the first switch and the first node, and secondly charging the panel capacitance through said inductor while removing the stored energy from said inductor until the inductor current reaches zero or before zero via the first current path; and

(b) discharging the panel capacitance through said inductor initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum through a second current path formed via the panel capacitance, the first node, the second switch, the third node, the inductor and the second node, and secondly charging the panel capacitance through said inductor while removing the stored energy from said inductor until the inductor current reaches zero or before zero through the second current path.

20. The method of claim 19 further comprising:

maintaining panel capacitance after step (a) by a first clamping circuit having a third switch coupled to the first node and a first potential via a first conductive path; and

maintaining the panel capacitance after step (b) by a second clamping circuit having a fourth switch coupled to the first node and a second potential via a second conductive path.

21. The method of claim 20, wherein storing and removing of stored energy in the inductor is based on an LC resonance frequency if the inductor current reaches zero.

22. The method of claim 20, wherein charging and discharging of the panel capacitance is not based on an LC resonance frequency via the first and second clamping circuit clamping the panel capacitance prior to the inductor current reaching zero.

23. The method of claim 22, wherein the first and second clamping circuits clamp the panel capacitance prior to the inductor current reaches zero.

24. The method of claim 22, wherein the second clamping circuit pre-stores energy in the inductor prior to step (a) and the first clamping circuit pre-stores energy in the inductor prior to step (b).

25. A plasma display panel driver circuit comprising:

a panel inter-electrode capacitor provided between at least one of a plurality of scanning electrodes and a plurality of sustain electrodes of a panel;

a charging/discharging circuit connected in series with said panel inter-electrode capacitor and between first and second nodes,

a clamping circuit having first and second switches for clamping a terminal voltage across the panel inter-electrode capacitor to a first power source voltage level and to a second power source voltage level, said first switch being connected in series between the first node and the first power source voltage level, said second switch being connected in series between said first node and the second power source voltage level,

said inter-electrode capacitor being connected in series to the first and second nodes and said charging/discharging circuit and said clamping circuit being coupled in parallel between the first and second nodes, wherein

said charging/discharging circuit comprises a pair of switches coupled in parallel to each other between the first anode and a third node and an inductive coil coupled in series between the second and third nodes.

26. The plasma display panel driver circuit of claim 25, wherein each of the pair of switches comprises a first transistor and a diode, and the pair of switches provide opposite current paths.

27. The plasma display panel driver circuit of claim 25, wherein the inter-electrode capacitor is charged/discharged based on an LC resonant frequency of the inductor coil and the inter-electrode capacitor.

28. The plasma display panel driver circuit of claim 25, wherein the inter-electrode capacitor is charge/discharged based on a non-LC resonant frequency of the inductor coil and the inter-electrode capacitor.

29. The plasma display panel driver circuit of claim 28, wherein the clamping circuit clamps the inter-electrode capacitor one of the first and second power source voltage level prior to an energy of the inductor coil reaching zero.

30. The plasma display panel driver circuit of claim 29, wherein the clamping circuit increases an energy of the inductor coil prior to charging/discharging of the inter-electrode capacitor.

31. The plasma display panel driver circuit of claim 25, wherein each of said first and second switches comprises a transistor.